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REGARDING:

Title:	LOCAL AND GLOBAL REGISTER PARTITIONING IN A VLIW PROCESSOR		
Application No.:	09/204,585	**Filed:**	December 3, 1998
Examiner:	David Y. Eng	**Group Art Unit:**	2155
Atty. Docket No.:	004-3288	**Confirmation No.:**	5684

ATTACHED HERETO:

(1) Reply Brief (8 pages)
(2) Transmittal Letter (1 page)

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David W. O'Brien — 10-Jan-05 (Date)

Respectfully submitted,

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Mail Stop Appeal
Commissioner for Patents
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Alexandria, VA 22313-1450

Applicant:	Marc Tremblay and William Joy		
Title:	LOCAL AND GLOBAL REGISTER PARTITIONING IN A VLIW PROCESSOR		
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Dear Sir:

Transmitted herewith are the following document(s) in the above-identified application:

(1) Reply Brief (8 page(s))
(2) This Transmittal Letter (1 page(s))

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Marc Tremblay and William Joy		
Title:	LOCAL AND GLOBAL REGISTER PARTITIONING IN A VLIW PROCESSOR		
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January 10, 2005

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REPLY BRIEF (37 C.F.R. § 41.41)

This brief is in response to Examiner's Answer, mailed November 8, 2004, which sets a period for reply ending January 10, 2005 (January 8 being a Saturday). Applicants respectfully request consideration of the following in connection with the present appeal.

In the Answer, Examiner (1) states that the *summary of invention* contained in Applicant's brief is deficient, (2) states that Applicant's *statement of issues* is incorrect and (3) contests *grouping* of claims, specifically asserting that certain claims stand or fall together. In response to Appellant's Brief, Examiner has withdrawn two (of the four) previously asserted *grounds of rejection*. Appellant thanks the Examiner for clearing the appeal of extraneous issues. Finally, Examiner responds to Appellant's argument. We take, in turn, each of the issues of apparent substantive disagreement.

SUMMARY OF INVENTION

Appellant has reviewed the observations in Examiner's Answer and notes that two competing usages of the term N have apparently been a source of confusion. Unfortunately, the reformulation of the expression for total number of registers proposed in the Examiner's Answer is *not* correct.

For avoidance of doubt, Appellant provides below a *revised* Summary of the Invention. The revised text eliminates the competing (and apparently confusing) usages of N. The revised text is now consistent with the claims on appeal and with description of the Application as filed.

As now revised, the summary of invention (previously included in the Appeal Brief) is correct and complies with 37 C.F.R. § 1.192, which controls based the date the Appeal Brief was filed. Consistent with the description of the Application as filed and the Summary of Invention included with the Appeal Brief, N_G is the total number of global registers addressable (e.g., after partition of register file segments); N_L is the total number of local registers addressable by a given functional unit (e.g., after partition). Accordingly, N_G+N_L is the number of registers (global and local) addressable by a given functional unit and $N_G+(M*N_L)$ is the aggregate number of registers addressable by the M functional units.

SUMMARY OF INVENTION: This presently claimed invention relates to processors storing information in register files, and more particularly to processors employing register files divided into multiple register file segments each coupled to and associated with a respective functional unit, wherein each register file segment is partitioned (or partitionable) into local and global registers. The register file and/or register file segments thereof are implemented as an addressable array that is partitionable into global and local register portions. In some embodiments, such a partition is programmable.

Referring to Fig. 6, for example, a schematic block diagram shows a register file 600 for an exemplary very long instruction word (VLIW) processor 100 that includes an implementation of global and local register partitioning. The VLIW processor has a plurality of functional units including three media functional units 622, 624, and 626, and a general functional unit 620. The processor 100 also includes a multi-port register file 600 that is divided into a plurality of separate register file segments 610, 612, 614, and 616, each of the register file segments being associated to one of the plurality of functional units. The register file segments 610, 612, 614, and 616 are partitioned into local registers and global registers. The global registers are read and written by all functional units 620, 622, 624, and 626. The local registers are read and written only by a functional unit associated with a particular register file segment. The local registers

and global registers may be addressed using register addresses in an address space that is separately defined for a register file segment/functional unit pair including register file segment 610/general functional unit 620, register file segment 612/media functional unit 622, register file segment 614/media functional unit 624, and register file segment 616/media functional unit 626.

In one embodiment, the global registers are addressed within a selected global register range using the same register addresses for the plurality of register file segment/functional unit pairs, for example, global registers 0-95. The local registers in a register file segment are addressed using register addresses in a local register range outside the global register range, for example addresses 96-127, that are assigned within a single register file segment/functional unit pair. Register addresses 96-127 applied to the register file segments in the local register range are the same for the plurality of register file segment/functional unit pairs and address registers locally within a register file segment/functional unit pair. The register specifiers of the local registers, as defined external to the processor (e.g., by a compiler), do not overlap, but instead have distinct and different specifiers. For example, in one embodiment, 96 global registers are addressed using address specifiers 0-95 in all of the four register file segments. Local registers 96-127 in the register file segment 610, local registers 128-159 in register file segment 612, local registers 160-191 in register file segment 614, and local registers 192-223 in register file segment 616 are all addressed using register addresses 96-127. In this example, the total number of distinct and independent registers is 96+(4*32) = 224. The 224 registers are addressed using 7 bits that define an address space from 0-127, rather than the 8 bits that are otherwise required to access 224 registers. In a general case, the number of registers can be expressed as $N_G + (M*N_L) = K$, with the number of bits being used by any one functional unit to address N registers ($N=N_G+N_L$) being equal to the number of bits B that are used to address $N=2^B$.

In some VLIW exploitations, global and local register partitioning advantageously leverages the information content of register specifier bits in an instruction word by inherently communicating information by position dependence within a VLIW instruction group. The positioning of a register specifier in the instruction word thus communicates addressing information. The additional information allows a compiler or programmer to specify more

registers in fewer bits than have been specified conventionally. One address bit is thus saved for each of the four subinstruction positions, a savings of four bits per subinstruction and a savings of 16 bits per VLIW instruction. The reduction in address bits is highly advantageous in a VLIW processor that includes powerful functional units that execute a large plurality of instructions, each of which is to be encoded in the VLIW instruction word.

In general embodiments, the register file 600 includes K physical registers. The K-register register file 600 is implemented as M replicated register file segments 610, 612, 614, and 616, each having a reduced number of read and/or write ports in comparison to a nonreplicated register file, but each having the same number of physical registers. The register file segments are partitioned into N_G global and N_L local register files where N_G plus N_L is equal to N. The register file operates equivalently to having $N_G + (M^* N_L)$ total registers available for the M functional units. The number of address bits for addressing the $N_G + (M^* N_L)$ total registers remains equal to the number of bits B that are used to address $N=2^B$ registers. The local registers for each of the M register file segments are addressed using the same B-bit values.

In some embodiments, partitioning of the register file 600 is programmable so that the number N_G of global registers and number N_L of local registers is selectable and variable. For example, a register file including four register file segments each having 128 registers may be programmably configured as a flat register file with 128 global registers and 0 local registers with the 128 registers addressed using seven address bits. Alternatively, the four register file segments may be programmably configured, for example, to include 64 global registers and 64 local registers so that the total number of registers is 64+(4*64)=320 registers that are again addressed using 7 bits rather than the 9 bits that would otherwise be required to address 320 registers.

Suitable array configurations, decode logic, read and write port configurations, word and bit line configurations and other particulars for exemplary implementations of a register file (and individual segments thereof) are described in the specification in greater detail with reference to FIGS. 7, 8A, 8B and 9.

ISSUES

In a effort to aid this Honorable Board in the understanding of underlying substantive issues, Appellant has included with the statement of issues, a summary of points of substantive disagreement with respect to the scope and content of the prior art. Issues have been revised in view of Examiner's withdrawal of certain grounds of rejection. Appellants believe there is substantial agreement as to the sections of U.S. code and combinations of references relied upon by the Office. The issues are as follows:

1. ***QUESTION***: Are claims 1, 3-14 and 23-28 unpatentable under 35 U.S.C. §103(a) over U.S. Patent No. 5,592,679 (Yung) in view of U.S. Patent No. 5,911,149 (Luan)?

   ANSWER: No. As a first substantive matter, neither *Yung* nor *Luan*, taken alone or in combination, discloses or suggests register file segments each coupled to and associated with a respective functional unit and each implemented as an addressable array and partitionable into global and local registers. Accordingly, no *prima facie* case of obviousness has been made out. Second, no proper construction of *Luan* is consistent with an interpretation of *Luan's* configurable memory bank allocation technique as register file segments that are partitionable into global registers and local registers. Accordingly, *Luan* does not add disclosure missing from *Yung* and, even if combined with *Yung*, no *prima facie* case of obviousness has been made out. Third, memory banks are not registers and *Luan's* exploitation of selective allocation of memory banks is neither analogous to Applicant's programmable partitioning of a register file segment implemented as an addressable array, nor suitable for use in combination with *Yung*. Accordingly, it is improper to combine references in the way suggested by the Office.

2. ***QUESTION***: Are Claims 2, and 15-22 unpatentable under 35 U.S.C. §103(a) over U.S. Patent No. 5,592,679 (Yung) in view of U.S. Patent No. 5,911,149 (Luan), and further in view of 6,023,757 (Nishimoto)?

   ANSWER: No. As before, neither *Yung* nor *Luan*, taken alone or in combination, discloses or suggests register file segments each coupled to and associated with a

respective functional unit and each implemented as an addressable array and partitionable into global and local registers. *Nishimoto* does not add the missing disclosure and, indeed, the Office relies on *Nishimoto* only for the teaching of a VLIW-type processor. Accordingly, no *prima facie* case of obviousness has been made out. Further, since neither *Luan* nor *Nishimoto* adds the disclosure missing from *Yung*, even if combined with *Yung*, no *prima facie* case of obviousness has been made out. Finally, at least with respect to *Yung* and *Luan*, it is improper to combine references in the way suggested by the Office.

GROUPING OF CLAIMS

Examiner's apparent objections to the contrary, grouping of claims remains as stated in the Appeal Brief. Contrary to the assertions in Examiner's Answer, claims of groups 1 and 2 do *NOT* stand or fall together. Appellant's decision not to dispute a particular aspect of *Nishimoto's* teaching is simply not relevant to the grouping of claims. Claims of groups 1 and 2 are distinct; indeed, they were separately grouped and separately argued in the Appeal Brief. Claims of groups 1 and 2 do not stand or fall together. In addition, certain claims within group 2 (particularly claims 15 and 22) were separately argued in the Appeal Brief. Furthermore, claims of group 3 do *NOT* stand or fall together. Argument (in the Appeal Brief) clearly states that the basis for distinction argued with respect group 3 is "in addition to reasons previously given," i.e., separately argued in connection with claim 21 and claims 8 and 28.

Finally, it should be noted that since programmable partitionability has been separately argued (e.g., with respect to claim 22 of group 2), claim 9 (which, though ostensibly a group 1 claim, depends from claim 8 of group 3 and includes corresponding language related to programmable partitionability) should also be viewed as separately argued and standing or falling independent of other claims of group 1. To the extent necessary and proper, Appellant hereby states that claim 9 does not stand or fall with other claims of group 1.

ARGUMENTS IN REPLY

Substantive arguments laid out in the Appeal Brief establish the legal error represented by the present Final Rejection. However, several aspects of the Examiner's Answer bear comment.

(1) Novelty and Non-obviousness are properly evaluated by comparing the specific claim language with the express (and possibly inherent) disclosure of the relied upon references. Contrary to the Office's argument in response to Appellant's Brief, and without conceding the alleged similarity, it is important to note that similarity in "thrust" (or gist) of the claimed invention and any invention disclosed in a relied upon reference plays no role in proper legal analysis of obviousness. *See* MPEP 2141.02. Appellant's Brief details legally significant differences between Appellant's claims and the disclosure of relied upon references.

(2) Examiner's reasoning with respect to both partitioning and resulting numbers of global and local registers is colored by a fundamental misinterpretation of terms. In particular, statements B and D made in the Examiner's Answer at page 8 are simply incorrect. To the contrary, N_G is the total number of global registers addressable (e.g., after partition of the register file segments); N_L is the total number of local registers addressable by a given functional unit (e.g., after partition). Accordingly, N_G+N_L is the number of registers (global and local) addressable by a given functional unit and $N_G+(M*N_L)$ is the aggregate number of registers addressable by the M functional units.

(3) In an attempt to avoid the clear inapplicability of *Luan's* configurable memory bank structure to the claimed combination of register file segments each coupled to and associated with a respective functional unit and each implemented as an addressable array and partitionable into global and local registers, the Office seeks to analogize register and memory storage. However, in doing so, the Office trivializes the point. It is not that registers and memory encode fundamentally different types of data. Rather, the important point is that, properly construed, *Luan's* memory banks cannot

correspond to structures recited in the claims. Appellant's Brief details the differences.

CONCLUSIONS

For the reasons outlined herein and in the Appellant's Brief, the present rejection of claims 1-28 should be reversed. Accordingly, Appellant respectfully requests that this Honorable Board do so and direct the present application to be issued.

Respectfully submitted,

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